interlevel dielectric; and forming the borderless contact by filling the contact area with a material comprised of a metal.

[0014] In a further exemplary embodiment of the invention, a semiconductor device comprising: a substrate; and a gate structure on the substrate, the gate structure comprising a layer of semiconductor material overlying the substrate, a layer comprised of a metal overlying the layer of semiconductor material, a layer comprised of polycrystalline silicon overlying the layer comprised of a metal, a layer of silicide overlying the layer comprised of polycrystalline silicon and a cap layer overlying the layer of silicide.

[0015] In another exemplary embodiment of the invention, a semiconductor device comprising: a substrate; a gate structure on the substrate, the gate structure comprising a metal gate core that is adjacent to a layer of dielectric material on at least two surfaces of the metal gate core; and a cap layer overlying the layer of dielectric material and the metal gate core.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0016] The foregoing and other aspects of embodiments of this invention are made more evident in the following Detailed Description, when read in conjunction with the attached Drawing Figures, wherein:

[0017] FIG. **1** shows an exemplary, conventional multi-FET structure;

[0018] FIGS. **2-4** illustrate a conventional technique for forming a borderless contact in the multi-FET structure of FIG. **1**;

[0019] FIGS. **5-10** show a first technique for forming a borderless contact in a semiconductor device in accordance with a first exemplary embodiment of the invention;

[0020] FIGS. **11-19** illustrate a second technique for forming a borderless contact in a semiconductor device in accordance with a second exemplary embodiment of the invention;

[0021] FIGS. **20-26** depict a third technique for forming a borderless contact in a semiconductor device in accordance with a third exemplary embodiment of the invention;

[0022] FIGS. **27-31** show a fourth technique for forming a borderless contact in a semiconductor device in accordance with a fourth exemplary embodiment of the invention;

[0023] FIG. **32** depicts a flowchart illustrating one non-limiting example of a method for practicing the exemplary embodiments of this invention;

[0024] FIG. **33** shows a flowchart illustrating another non-limiting example of a method for practicing the exemplary embodiments of this invention;

[0025] FIG. **34** depicts a flowchart illustrating another non-limiting example of a method for practicing the exemplary embodiments of this invention;

[0026] FIG. **35** shows a flowchart illustrating another non-limiting example of a method for practicing the exemplary embodiments of this invention; and

[0027] FIG. **36** depicts a flowchart illustrating another non-limiting example of a method for practicing the exemplary embodiments of this invention.

DETAILED DESCRIPTION

1. Further Considerations

[0028] FIG. **1** shows an exemplary, conventional multi-FET structure **10**. The structure **10** includes a number of components or regions that are overlying or embedded in a substrate (SUB) **12**. There are STI regions **14** and source/drain regions (S/D) **16**. The S/D **16** lies below portions of the gates **18**. Each gate includes a number of layers (not labeled), such as: a dielectric layer (e.g., silicon oxide) overlying the substrate, a poly layer overlying the dielectric layer and a cap layer (e.g., nitride) overlying the poly. Surrounding each gate **18** are spacers (SPA) **20**. The SPA **20** and the nitride cap protect the other layers of the gate **18** from undesired contacts and shorts. To reduce resistance, there may be a layer of silicide (SIL) **22** over the S/D **16**.

[0029] FIGS. **2-4** illustrate a conventional technique for forming a borderless contact in the multi-FET structure of FIG. **1**. As shown in FIG. **2**, an interlevel dielectric (ILD) **24** (e.g., an oxide) is deposited over the structure **10**. In FIG. **3**, the contact is formed by patterning and RIE. To form the borderless contact, the etched region is filled with a metal at the CA **26**, as depicted in FIG. **4**.

[0030] In some cases, conventional techniques may result in a damaged spacer, for example, due to source/drain ion implantation, CA RIE or cleaning. Such a damaged spacer can cause electrical shorts between gate and CA contacts, for example. Furthermore, thick spacers for the silicide formation and a tight pitch may result in a small CA space, leading to a more difficult CA fill. In addition, the nitride spacer has a high parasitic capacitance, inhibiting operation of the final structure.

[0031] As noted above, device scaling results in a small space for forming the borderless contact. Pitch scaling means there is a narrower space for the CA and a bordered contact will not work. For example, consider a 22 nm node having a pitch of 80 nm, a gate length of about 25 nm and a spacer thickness of about 18 nm per side. This leaves about 19 nm of space for the CA (80−25−2×18=19) which is too small for a bordered contact. Furthermore, and also as noted above, conventional borderless contact techniques have various problems. Therefore, further techniques are needed that improve upon conventional borderless contact techniques.

2. Various Exemplary Embodiments of the Invention

[0032] The exemplary embodiments of the invention provide a number of improvements over conventional borderless contacts and conventional borderless contact techniques. Some of the exemplary embodiments seek to address and improve upon the above-noted shortcomings in prior art systems.

[0033] A first exemplary embodiment of the invention provides for replacement of the spacers after the contact via etch. As a non-limiting example, the replacement spacers may be low-k spacers to reduce the parasitic capacitance. The first exemplary embodiment also provides for formation of a second set of spacers above the cap of the gate (e.g., above the nitride cap and adjacent to the ILD). This second set of spacers may also be low-k spacers.

[0034] Various further exemplary embodiments of the invention describe how at least a portion of the gate is removed after deposition and planarization of the ILD. A second exemplary embodiment applies a borderless contact technique to a gate-first metal/poly/silicide gate stack. A cap layer (e.g., a nitride cap) is removed in order to enable the formation of silicide on the gate structure (e.g., overlying a poly layer). Another cap layer (e.g., a nitride cap) is then formed (e.g., overlying the silicide layer) by deposition and planarization.